10.5 A 58-to-60.4GHz Frequency Synthesizer in 90nm CMOS

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The mm-wave band of 57 to 64GHz has been announced for the general unlicensed use and it may facilitate the multi-Gb/s wireless transmission for short distance indoor communications. In such wireless transceivers, the very-high-speed frequency synthesizer plays an important role. In this paper, a 58-to-60.4GHz frequency synthesizer that is implemented in a 90nm CMOS technology is presented.

The proposed frequency synthesizer is shown in Fig. 10.5.1. In this figure, f_{div} and f_{ref} denote the frequency of CK_{div} and CK_{ref}. The harmonic-locked phase detector (PD) and frequency detector (FD) are adopted to reduce the spur and speed up the settling time. The voltage-controlled oscillator (VCO) with a distributed *LC* tank and the current-reuse split-load frequency divider are proposed to achieve the high-frequency operation. Moreover, a dual-modulus divide-by-128/129 prescaler and the on-chip loop filter are also adopted. The circuit details are discussed as follows:

It is well-known that the active devices in advanced CMOS technologies suffer from the gate leakage and the channel-length modulation due to the thinner gate oxide thickness and the shorter channel length [1]. These may cause some issues for the very high-frequency VCO design. Firstly, to have a wide tuning range for a VCO, a large varactor is often used. However, the parasitic capacitance limits the oscillation frequency and the gate leakage current degrades the phase noise. Secondly, since the cross-coupled devices with short channel lengths may offer the finite output resistance, the equivalent quality factor from the *LC* tank is decreased. It also degrades the phase noise performance and even stops the oscillation of the VCO. To overcome the above problems, the proposed VCO with a distributed *LC* tank is shown in Fig. 10.5.2. The layout for four inductors is also shown in Fig. 10.5.2. The inductors, L_1 and L_4, are used to resonate with the parasitic capacitances of the cross-coupled devices. It enhances the oscillation frequency and impedance of the output. To reduce the leakage, a small varactor is used instead of a large varactor. To have a wide tuning range, the metal capacitors, controlled by three switches *SW,* are used in Fig. 10.5.2. While this VCO drives the divider and the instrument with a 50Ω load, two independent buffers are used.

To tolerate the impact of process and temperature variations on the performance of a VCO, the frequency divider with a wide operational range is needed. Figure 10.5.3 shows the proposed current-reuse latch. A conventional current-mode logic (CML) latch requires the input clocking transistor to have large widths or large dc bias currents to operate at very high frequency. In this proposed latch, the transistors $M_{5\text{-}6}$ are added to increase the total transconductance of the input clocking transistor, based on the current-reuse technique. In addition, it decreases the bias current of $M_{1\text{-}4}$ to enhance the switching speed. The split-load technique [2] is also used to extend the operational frequency range compared with the conventional shunt-peaking technique. To realize the static divide-by-2 divider, the master and slave latches are used. Simulation results show that the divide-by-2 divider using the proposed latches operates in the frequency range of 43 to 71GHz from an input power of 0dBm while drawing 9.2mA from a 1.2V supply.

The dual-modulus divide-by-128/129 prescaler consists of a synchronous divide-by-4/5 circuit and an asynchronous divide-by-32 circuit, which is realized by cascading five divide-by-2 dividers. To achieve a high-speed divide-by-4/5 prescaler, the merged NOR-DFF circuit is used to replace the cascade of a NOR gate and a DFF [3]. It reduces the gate delay to enhance the operating speed. Note that this prescaler adopts the CML circuits without passive inductors.

Figure 10.5.4 shows the single-ended harmonic-locked PD and its timing diagram. In fact, the differential CML circuits are used to realize the proposed PD. As shown in Fig. 10.5.1, the feedback clock CK_{div} comes from the penultimate DFF of the asynchronous divide-by-32 circuit instead of the last one. The feedback clock CK_{div} with twice the frequency of the reference clock CK_{ref} (i.e.,) is treated as the down signal "*DN*". The up signal "*UP*" is generated by an XOR gate and a DFF as shown in Fig. 10.5.4. The timing diagrams for the early, late, and lock conditions of the PD are shown in Fig. 10.5.4. For example, it can be seen from this figure that the equivalent frequency of the up/down signals is twice that of the reference clock in the lock condition. The conventional FD [4] is used because it also locks at harmonic frequency. By using the harmonic PD/FD, it achieves a low reference spur and fast settling time owing to the equivalent higher input frequency. The voltage-to-current converter (V/I) [4] is also used to convert the phase/frequency error into a voltage to control the VCO via on-chip loop filter.

The frequency synthesizer is fabricated in a 90nm CMOS technology. Figure 10.5.5 shows the die micrograph which occupies 0.95×1mm^2 with a 3rd-order loop filter and pads. It consumes 80mW from 1.2V supply with buffers. The measured performance results of the synthesizer are summarized in Fig. 10.5.6 and compared with previous work. While the controlled signal SW is on and off, the measured VCO tuning range is 57.9 to 59.4GHz and 59 to 60.5GHz, respectively. Figure 10.5.7 shows the measured spectra of 59.93GHz and 60.4GHz for f_{ref} = 234.1MHz and the divide ratio of 256 and 258, respectively. The measured reference spur is –50.75dBc and –50.4dBc at correspondingly 59.93GHz and 60.4GHz. For 60.4GHz, the measured phase noise at 1MHz (2MHz) offset is –85.1dBc/Hz (–95dBc/Hz). The measured frequency hopping time is less than 1.6μs, while switching from 59.93GHz to 60.4GHz.

Moreover, for f_{ref} = 230MHz and the divide ratio of 256 (258), the measured output frequency is 58.88GHz (59.34GHz). The measured reference spur is –52.09dBc and –53.71dBc at 58.88GHz and 59.34GHz, respectively. The whole operation frequency of this synthesizer is measured from 58GHz to 60.4GHz.

Acknowledgements:
The authors would like to thank TSMC, Hsinchu, Taiwan to fabricate this chip and Agilent Technologies, Taiwan, to support the measurement. This work is also supported in part by MediaTek and NSC, Taiwan.

References:
[1] J. Pineda de Gyvez and H.P. Tuinhout, "Threshold Voltage Mismatch and Intra-Die Leakage Current in Digital CMOS Circuits," *IEEE J. Solid-State Circuits*, vol. 39, pp. 157-168, Jan., 2004.
[2] C. Lee, L.C. Cho, and S.I. Liu, "A 1.2V 37-38.5GHz 8-Phase Clock Generator in 0.13μm CMOS Technology," *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 34-35, June, 2006.
[3] C. Lee, L.C. Cho, and S.I. Liu, "A 44GHz Dual-Modulus Divide-by-4/5 Prescaler in 90nm CMOS Technology," *Proc. IEEE CICC*, pp. 397-400, Sept., 2006.
[4] R.C.H. van de Beek, C.S. Vaucher, D.M.W. Leenaerts, et al.,"A 2.5 to 10GHz Clock Multiplier Unit with 0.22ps rms Jitter in a 0.18μm CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 178-179, Feb., 2003.
[5] W. Winkler, J Borngraber, B Heinemann, et al., "A Fully Integrated BiCMOS PLL for 60GHz Wireless Applications," *ISSCC Dig. Tech. Papers*, pp. 406-407, Feb., 2005.
[6] J. Jeong and Y. Kwon, "A Fully Integrated V-Band PLL MMIC Using 0.15μm GaAs pHEMT Technology," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1042-1050, May, 2006.

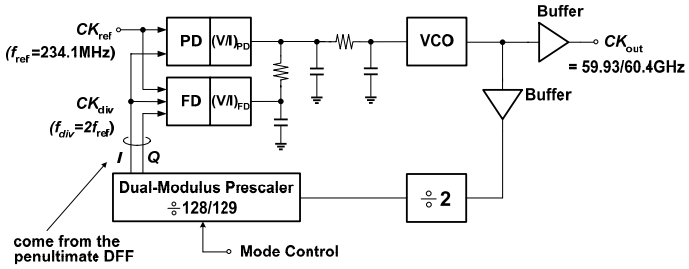

Figure 10.5.1: The proposed frequency synthesizer.

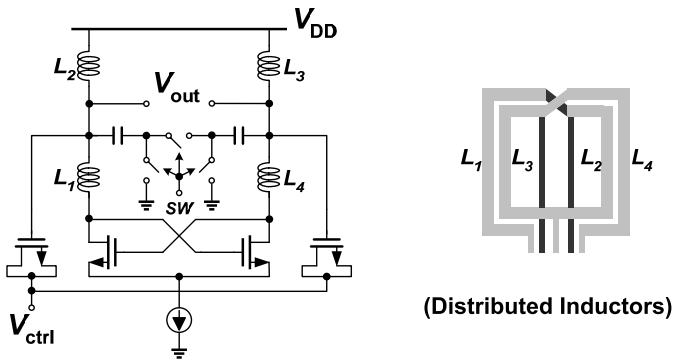

Figure 10.5.2: The proposed VCO.

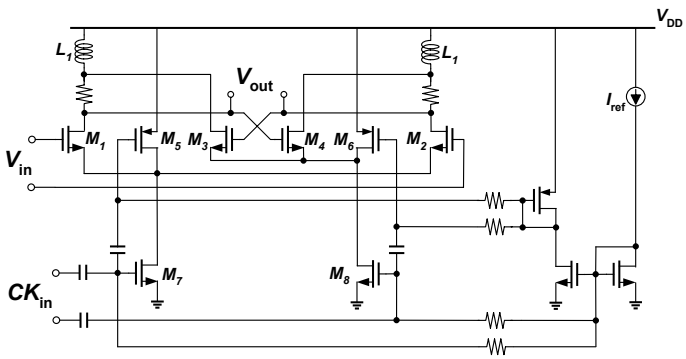

Figure 10.5.3: The proposed current-reuse latch.

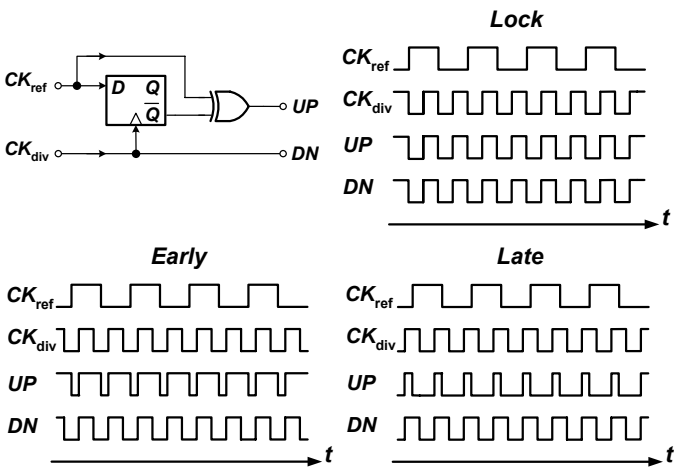

Figure 10.5.4: The proposed PD and its timing diagram.

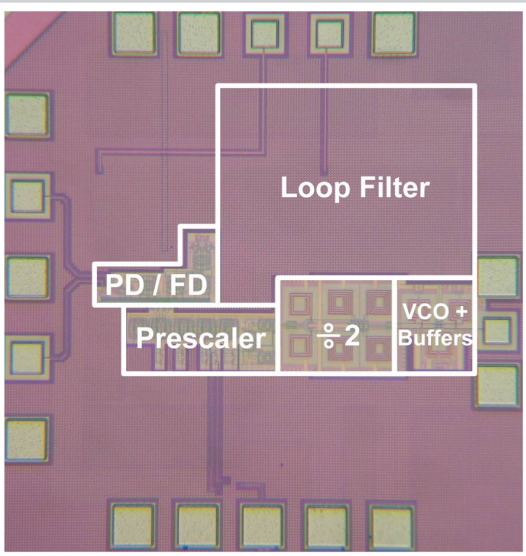

Figure 10.5.5: Die micrograph.

	[5]	[6]	This Work
Technology	SiGe 0.25um	GaAs 0.15μm	CMOS 90nm
Type	PLL	PLL	Frequency Synthesizer
Lock Range	54.5-57.8GHz	60-60.8GHz	58-60.4GHz
Divide Ratio	1024	12	256/258
Supply	3V	5V	1.2V
Power	650mW	370mW	80mW
Chip Area	0.8 mm²	1.8×2.35 mm²	0.95×1 mm²
Ref. Spur	-50.5dBc @57.34GHz	N/A	-50.75dBc @59.93GHz -50.40dBc @60.4GHz
Phase Noise	N/A	-95.5dBc/Hz @100kHz -112.4dBc/Hz @ 1MHz @60GHz	-85.1dBc/Hz @ 1MHz -95.0dBc/Hz @ 2MHz @60.4GHz

Figure 10.5.6: Measured performance summary and comparison.

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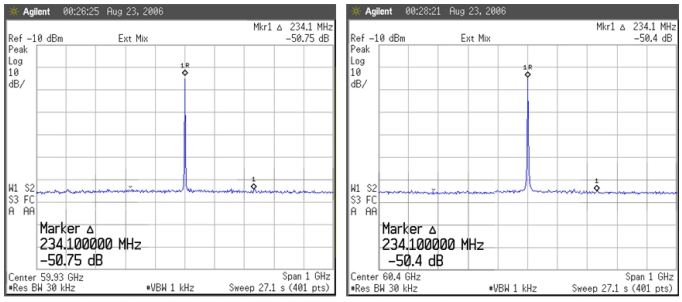

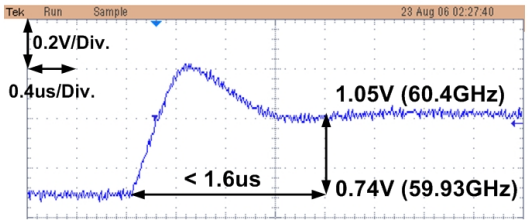

Figure 10.5.7: The measured spectra and hoping behavior of the synthesizer.

